

What Is Claimed Is:

1. A method for manufacturing a semiconductor device,  
comprising the steps of:  
defining gate electrode and capacitor regions by adapting a  
5 photoetching process to a semiconductor substrate deposited with a gate oxide film  
and a gate poly, so that the distance between the gate electrode region and the  
capacitor region can be smaller than twice the thickness of a spacer to be formed later;  
growing an oxide film on top of the gate poly and defining a LDD  
region using phosphor (P) as impurities;  
10 forming a spacer by depositing and etching an oxide film on the  
sidewalls of the gate oxide film and gate poly where the gate electrode and capacitor  
regions are defined;  
implanting a high concentration As on the surfaces of a bit line contact  
junction and a gate poly formed between the gate electrodes by implanting a high  
15 concentration As to the surface of the resulting material with the spacer; and  
implanting phosphor (P) as impurities so as to surround the region  
implanted with As.
2. The method of claim 1, wherein the step of defining the LDD  
20 region is carried out by implanting phosphor with a concentration of  $5 \times 10^{13}$   
atoms/cm<sup>2</sup> at a depth of about 200Å.
3. The method of claim 2, wherein the step of implanting  
phosphor as impurities so as to surround the region implanted with As is carried out  
25 by implanting phosphor with a concentration of  $5 \times 10^{13}$  atoms/cm<sup>2</sup> at a depth of about  
600Å.
4. The method of claim 1, wherein the distance between the gate  
electrode region and the capacitor region is smaller than 0.26µm.

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5. A method for manufacturing a semiconductor device,  
comprising the steps of:

defining gate electrode and capacitor regions by adapting a  
photoetching process to a semiconductor substrate deposited with a gate oxide film  
5 and a gate poly, so that the distance between the gate electrode region and the  
capacitor region can be smaller than twice the thickness of a spacer to be formed later;  
growing an oxide film on top of the gate poly and defining a first LDD  
region using as impurities;  
forming a spacer by depositing and etching an oxide film on the  
10 sidewalls of the gate oxide film and gate poly where the gate electrode and capacitor  
regions are defined; and  
implanting a high concentration As one more time on the surfaces of a  
bit line contact junction and a gate poly formed between the gate electrodes by  
implanting a high concentration As to the surface of the resulting material with the  
15 spacer; and  
wherein the method further comprises the step of forming a second  
LDD region so as to surround the first LDD region using phosphor (P) as impurities  
after carrying out the step of defining the first LDD region.

20 6. The method of claim 5, wherein the step of defining the second  
LDD region using phosphor is carried out by implanting the phosphor at a depth of  
500Å.

25 7. The method of claim 5, wherein the distance between the gate  
electrode region and the capacitor region is smaller than 0.26µm.